

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

- 1 1. (Amended) A test pattern generation and comparison apparatus in
2 communication with a built-in-self-test controller and functional integrated
3 circuits , comprising:
4 a background and command decoder connected to receive test
5 background and command codes from said test controller, to
6 translate said test background and command codes to multiple bit
7 test stimulus signals that, when applied to said functional integrated
8 circuits, create test response signals from said functional integrated
9 circuits, ~~whereby said test stimulus signal has a plurality of bits; and~~
10 a plurality of latency buffers connected to said background and
11 command decoder to receive said multiple bit test stimulus signals
12 and to adjust in time the relationship of the bits of said multiple bit
13 test stimulus signals as required by said functional integrated
14 circuits.

- 1 2. (Amended) The test pattern generation and comparison apparatus of
2 claim 1 further comprising:

3 a plurality of parallel-to-serial converters, ~~wherein each parallel-to-~~
4 serial converter is connected to one of the plurality of latency
5 buffers, to convert said multiple bit test stimulus signals to a
6 serialized multiple bit test stimulus signals to be scanned to a scan
7 register of said functional integrated circuit.

1 3. (Amended) The test pattern generation and comparison apparatus of
2 claim 1 wherein said background and command decoder comprises:

3 high level command bus decode logic ~~which decodes a high level~~
4 ~~command bus~~ for activating RAM control signals, ~~and whereby the~~
5 ~~decode logic also controls the transfer of the~~ for controlling transfer
6 of a background pattern of expected results to the error control
7 module.

1 4. (Amended) The test pattern generation and comparison apparatus of
2 claim 1 wherein said latency buffer comprises:

3 a plurality of serially connected flip-flop circuits, ~~whereby~~ connected
4 such that a first flip-flop circuit of said plurality of serially connected
5 flip-flop circuits has a data input connected to said background and
6 command decoder to receive one bit of said multiple bit test
7 stimulus signal and an output connected to a subsequent flip-flop
8 circuit of the serially connected flip-flop circuits, ~~whereby and~~
9 connected such that each subsequent flip-flop circuit of the serially

10 connected flip-flop circuits has an output connected to the input of a
11 following flip-flop circuit of said plurality of serially connected flip-
12 flop circuits, and ~~whereby~~ connected such that a last flip-flop circuit
13 has an input connected to an output of a previous flip-flop circuit
14 and an output containing a delayed bit of said multiple bit test
15 stimulus signal.

1 5. (Amended) The test pattern generation and comparison apparatus of
2 claim 4 ~~whereby~~ wherein the adjusting in time of the bits of the serialized
3 multiple bit test stimulus signals is determined by a number of flip-flop
4 circuits in the plurality of serially connected flip-flop circuits and the
5 number of latency buffers of the plurality of latency buffers is determined
6 by a number of bits in the multiple bit test stimulus signals and a period of
7 a test access clocking signal.

1 6. (Original) The test pattern generation and comparison apparatus of claim
2 5 wherein the number of flip-flop circuits is determined by the formula

3
$$N = \frac{\lambda}{\phi}$$

4 where:

5 **N** is the number of said flip-flop circuits,

6 λ is the adjusting in time, and

ϕ is the period of the test access clocking
signal.

7. (Amended) The test pattern generation and comparison apparatus of
claim 2 wherein the parallel-to-serial circuit comprises:

a first plurality of flip-flops, ~~whereby each flip-flop has~~ having a data
input to receive one of a first portion of bits of said multiple bit test
stimulus signal and a clock input ~~to receive~~ receiving a clocking
signal to latch said the bit of the multiple bit test stimulus signal;

a first plurality of multiplexor circuits, ~~whereby each multiplexor circuit~~
~~has~~ having a first input to receive one of a remaining portion of bits
of said multiple bit test stimulus signal, second input to receive an
output of one of the first plurality of flip-flops, and a select input to
receive a loading signal to selectively transfer the remaining bit of
the multiple bit test stimulus signal and the output of one of the first
plurality of flip-flops to an output of said multiplexor circuit;

a second plurality of flip-flops, ~~whereby each flip-flop of said plurality of~~
flip-flops has a data input connected to an output of one of the first
plurality of multiplexor circuits, and a clock input connected to
receive the clocking signal to latch the output of one of the first
plurality of multiplexor circuits to the output of said flip-flop of said
plurality of flip-flops; and

20 a second plurality of multiplexor circuits ~~whereby~~ each multiplexor
21 circuit ~~has~~ having a first input connected to a first flip-flop of the
22 plurality of flip-flops, second input connected to a second flip-flop of
23 the second plurality of flip-flops, and a select input connected to the
24 clocking signal to alternately transfer the first input to an output of
25 said multiplexor circuits and the second input to the output, as said
26 clocking signal changes from a first level to a second level and from
27 the second level to the first level.

1 8. (Amended) The test pattern generation and comparison apparatus of
2 claim 1 further comprising:

3 a test response comparison circuit connected to said background and
4 control decoder to receive an expected test response signal
5 providing a correct response expected from said integrated circuits
6 in response to said serialized multiple bit test stimulus signals, and
7 connected to said integrated circuit to receive a test response
8 signal that is the response of the integrated circuit to said serialized
9 multiple bit test stimulus signal.

1 9. (Amended) The test pattern generation and comparison apparatus of
2 claim 8 wherein the test response comparison circuit comprises:

3 a comparator circuit to receive the test response signal and the
4 expected test response signal, compare said test response signal

5 to said expected serialized test response signal and produce a test
6 results signal indicating functioning of said integrated circuits.

1 10. (Amended) The test pattern generation and comparison apparatus of
2 claim 9 wherein said comparator circuit comprises:

3 [[An]] an exclusive OR and OR logic tree which compares the RAM
4 ~~data output from the serial to parallel converter~~ test response signal
5 to an expected ~~data output pattern~~ test response signal from the
6 background data.

1 11. (Amended) The test pattern generation and comparison apparatus of
2 claim 9 wherein said test response comparison circuit further comprises:

3 a error-handling module ~~to that~~ receives the test response signal and
4 the expected test response signal and creates a diagnostic signal
5 indicating a location of any fault determined to exist within said
6 integrated circuits.

1 12. (Amended) The test pattern generation and comparison apparatus of
2 claim 11 wherein said error handling module comprises:

3 a serial shift register composed of flip-flops, ~~which that~~ are presettable
4 from the ~~serial to parallel data bus from the RAM~~ test response
5 signal, and said serial shift register ~~is being~~ loaded by the
6 ~~PASS/FAIL test result~~ signal from the comparator circuit, and

7 ~~whereby the~~ for transfer from a serial output ~~from of the~~ serial shift
8 register ~~transfers the data for~~ diagnosis.

1 13. (Amended) The test pattern generation and comparison apparatus of
2 claim 5 wherein a hardware description of said test pattern generation and
3 comparison apparatus requires the number of bits of the multiple bit test
4 stimulus signal and the adjusting in time of the multiple bit test stimulus
5 signal as parameters to automatically create a physical description of said
6 test pattern generation and comparison apparatus during an automatic
7 physical design of said integrated circuit for placement on said
8 semiconductor substrate.

1 14. (Original) The test pattern generation and comparison apparatus of claim
2 1 wherein said functional integrated circuits are selected from a group of
3 functional integrated circuits consisting of logic circuits and memory array
4 circuits.

1 15. (Amended) A built-in-self test circuit incorporated with functional integrated
2 circuits on a semiconductor substrate to verify correctness of operation of
3 said functional integrated circuits, comprising:

4 a built-in-self-test controller to provide test background and command
5 codes indicating tests to be performed on said functional integrated
6 circuits; and

7 a test pattern generation and comparison apparatus in communication
8 with the built-in-self-test controller to receive said test background
9 and command codes and with said functional integrated circuits to
10 transmit at least one test stimulus signal to said integrated circuit
11 and to receive at least one test response signal to evaluate
12 correctness of operation of said integrated circuit, comprising:

13 a background and command decoder connected to receive
14 said test background and command codes from said test
15 controller, to translate said test background and
16 command codes to multiple bit test stimulus signals that,
17 when applied to said functional integrated circuits, create
18 said test response signals from said functional integrated
19 circuits, ~~whereby said test stimulus signal has a plurality~~
20 ~~of bits~~; and

21 a plurality of latency buffers connected to said background
22 and command decoder to receive said multiple bit test
23 stimulus signals and to adjust in time the relationship of
24 the bits of said multiple bit test stimulus signals as
25 required by said functional integrated circuits.

1 16. (Amended) The built-in-self test circuit of claim 15 further comprising:

2 a plurality of parallel-to-serial converters wherein each parallel-to-serial
3 converter is connected to one of the plurality of latency buffers, to
4 convert said multiple bit test stimulus to a serialized multiple bit test
5 stimulus signals to be scanned to a scan register of said functional
6 integrated circuit.

1 17. (Amended) The built-in-self test circuit of claim 15 wherein said
2 background and command decoder comprises:

3 high level command bus decode logic ~~which decodes a high level~~
4 ~~command bus for activating RAM control signals, and whereby the~~
5 ~~decode logic also controls the transfer of the background pattern for~~
6 controlling transfer of a background pattern of expected results to
7 the error control module.

1 18. (Amended) The built-in-self test circuit of claim 15 wherein said latency
2 buffer comprises:

3 a plurality of serially connected flip-flop circuits, whereby connected
4 such that a first flip-flop circuit of said plurality of serially connected
5 flip-flop circuits has a data input connected to said background and
6 command decoder to receive one bit of said multiple bit test
7 stimulus signal and an output connected to a subsequent flip-flop
8 circuit of the serially connected flip-flop circuits, whereby connected
9 such that each subsequent flip-flop circuit of the serially connected

10 flip-flop circuits has an output connected to the input of a following
11 flip-flop circuit of said plurality of serially connected flip-flop circuits,
12 and ~~whereby~~ connected such that a last flip-flop circuit has an input
13 connected to an output of a previous flip-flop circuit and an output
14 containing a delayed bit of said multiple bit test stimulus signal.

1 19. (Amended) The built-in-self test circuit of claim 18 ~~whereby~~ wherein the
2 adjusting in time of the multiple bit test stimulus signals is determined by a
3 number of flip-flop circuits in the plurality of serially connected flip-flop
4 circuits and the number of latency buffers of the plurality of latency buffers
5 is determined by a number of bits in the multiple bit test stimulus signals.

1 20. (Original) The built-in-self test circuit of claim 19 wherein the number of
2 flip-flop circuits is determined by the formula:

$$N = \frac{\lambda}{\phi}$$

4 where:

5 **N** is the number of said flip-flop circuits,

6 λ is the adjusting in time, and

7 ϕ is the period of the test access clocking
8 signal.

1 21. (Amended) The built-in-self test circuit of claim 16 wherein the parallel-to-
2 serial circuit comprises:

3 a first plurality of flip-flops, ~~whereby~~ each flip-flop ~~has~~ having a data
4 input to receive one of a first portion of bits of said multiple bit test
5 stimulus signal and a clock input to receive a clocking signal to
6 latch said first portion of the bits of the multiple bit test stimulus
7 signal;

8 a first plurality of multiplexor circuits, ~~whereby~~ each multiplexor circuit
9 ~~has~~ having a first input to receive one of a remaining portion of bits
10 of said multiple bit test stimulus signal, second input to receive an
11 output of one of the first plurality of flip-flops, and a select input to
12 receive a loading signal to selectively transfer the remaining bit of
13 the multiple bit test stimulus signal and the output of one of the first
14 plurality of flip-flops to an output of said multiplexor circuit;

15 a second plurality of flip-flops, ~~whereby~~ each flip-flop of said plurality of
16 flip-flops ~~has~~ having a data input connected to an output of one of
17 the first plurality of multiplexor circuits, and a clock input connected
18 to receive the clocking signal to latch the output of one of the first
19 plurality of multiplexor circuits to the output of said flip-flop of said
20 plurality of flip-flops; and

21 a second plurality of multiplexor circuits, ~~whereby~~ each multiplexor
22 circuit ~~has~~ having a first input connected to a first flip-flop of the
23 plurality of flip-flops, second input connected to a second flip-flop of
24 the second plurality of flip-flops, and a select input connected to the
25 clocking signal to alternately transfer the first input to an output of
26 said multiplexor circuits and the second input to the output, as said
27 clocking signal changes from a first level to a second level and from
28 the second level to the first level.

1 22. (Amended) The built-in-self test circuit of claim 15 further comprising:

2 a test response comparison circuit connected to said background and
3 control decoder to receive an expected test response signal
4 providing a correct response expected from said integrated circuits
5 in response to said serialized multiple bit test stimulus signals, and
6 connected to said integrated circuit to receive a test response
7 signal that is the response of the integrated circuit to said serialized
8 multiple bit test stimulus signal.

1 23. (Original) The built-in-self test circuit of claim 22 wherein the test response
2 comparison circuit comprises:

3 a comparator circuit to receive the test response signal and the
4 expected test response signal, compare said test response signal

5 to said expected test response signal and produce a test results
6 signal indicating functioning of said integrated circuits.

1 24. (Amended) The built-in-self test circuit of claim 23 wherein said
2 comparator circuit comprises:

3 an exclusive OR and OR logic tree which compares the ~~RAM data~~
4 ~~output from the serial to parallel converter~~ test response signal to
5 ~~an expected data output pattern~~ test response signal from the
6 background data.

1 25. (Original) The built-in-self test circuit of claim 22 wherein said test
2 response comparison circuit further comprises:

3 a error-handling module to receive the test response signal and the
4 expected test response signal and creates a diagnostic signal
5 indicating a location of any fault determined to exist within said
6 integrated circuits.

1 26. (Amended) The built-in-self test circuit of claim 25 wherein said error
2 handling module comprises:

3 a serial shift register composed of flip-flops, ~~which that~~ are presettable
4 ~~from the serial to parallel data bus from the RAM~~ test response
5 signal, and said serial shift register ~~is being~~ loaded by the
6 ~~PASS/FAIL test result~~ signal from the comparator, ~~and whereby the~~

7 for transfer from a serial output from of the serial shift register
8 ~~transfers the data~~ for diagnosis.

1 27. (Amended) The built-in-self test circuit of claim 20 wherein a hardware
2 description of said built-in-self test circuit requires the number of bits of the
3 multiple bit test stimulus signal and the adjusting in time of the multiple bit
4 test stimulus signal as parameters to automatically create a physical
5 description of said built-in-self test circuit during an automatic physical
6 design of said integrated circuit for placement on said semiconductor
7 substrate.

1 28. (Original) The built-in-self test circuit of claim 15 wherein said functional
2 integrated circuits are selected from a group of functional integrated
3 circuits consisting of logic circuits and memory array circuits.

1 29. (Amended) A computer implemented hardware design system description
2 ~~coding providing a description of a computer implemented having a code~~
3 retention device retaining a hardware description coding of a test pattern
4 generation and comparison circuit, which, when executed, to automatically
5 creates a physical description of said ~~computer implemented hardware~~
6 description coding during an automatic physical design of ~~said an~~
7 integrated circuit for placement on ~~said a~~ semiconductor substrate,
8 ~~whereby said computer implemented hardware description coding~~
9 ~~comprises~~ comprising:

10 a descriptive coding of a background and command decoder
11 connected to receive test background and command codes from
12 said test controller, to translate said test background and command
13 codes to multiple bit test stimulus signals that, when applied to said
14 functional integrated circuits, create test response signals from said
15 functional integrated circuits, ~~whereby said test stimulus signal has~~
16 ~~a plurality of bits; and~~
17 a descriptive coding of a plurality of latency buffers connected to said
18 background and command decoder to receive said multiple bit test
19 stimulus signals and to adjust in time the relationship of each bit of
20 said multiple bit test stimulus signals as required by said functional
21 integrated circuits.

1 30. (Amended) The computer implemented hardware design system
2 ~~description coding~~ of claim 29 wherein the hardware description coding
3 ~~further comprising comprises:~~
4 a descriptive coding of a plurality of parallel-to-serial converters,
5 ~~wherein each parallel-to-serial converter is connected to one of the~~
6 plurality of latency buffers, to convert said multiple bit test stimulus
7 to a serialized multiple bit test stimulus signals to be scanned to a
8 scan register of said functional integrated circuit.

1 31. (Amended) The computer implemented hardware design system
2 ~~description coding~~ of claim 29 wherein said descriptive coding of said
3 background and command decoder comprises:

4 descriptive coding of high level command bus decode logic ~~which~~
5 ~~decodes a high level command bus for activating RAM control~~
6 ~~signals, and whereby the decode logic also controls the transfer of~~
7 ~~the~~ for controlling transfer of a background pattern of expected
8 results to the error control module.

1 32. (Amended) The computer implemented hardware design system
2 ~~description coding~~ of claim 29 wherein said a descriptive coding of the
3 latency buffer comprises:

4 a descriptive coding of a plurality of serially connected flip-flop circuits,
5 ~~whereby connected such that~~ a first flip-flop circuit of said plurality
6 of serially connected flip-flop circuits has a data input connected to
7 said background and command decoder to receive one bit of said
8 multiple bit test stimulus signal and an output connected to a
9 subsequent flip-flop circuit of the serially connected flip-flop circuits,
10 ~~whereby connected such that~~ each subsequent flip-flop circuit of
11 the serially connected flip-flop circuits has an output connected to
12 the input of a following flip-flop circuit of said plurality of serially
13 connected flip-flop circuits, and ~~whereby connected such that~~ a last

14 flip-flop circuit has an input connected to an output of a previous
15 flip-flop circuit and an output containing a delayed bit of said
16 multiple bit test stimulus signal.

1 33. (Amended) The computer implemented hardware design system
2 ~~description coding~~ of claim 32 ~~whereby~~ wherein the adjusting in time of the
3 multiple bit test stimulus signals is determined by a number of flip-flop
4 circuits in the plurality of serially connected flip-flop circuits and the
5 number of latency buffers of the plurality of latency buffers is determined
6 by a number of bits in the multiple bit test stimulus signals.

1 34. (Amended) The computer implemented hardware design system
2 ~~description coding~~ of claim 33 wherein the number of flip-flop circuits is
3 determined by the formula:

$$N = \frac{\lambda}{\phi}$$

5 where:

6 **N** is the number of said flip-flop circuits,

7 λ is the adjusting in time, and

8 ϕ is the period of the test access clocking
9 signal.

1 35. (Amended) The computer implemented hardware design system
2 ~~description coding~~ of claim 30 wherein the parallel-to-serial circuit
3 comprises:

4 a descriptive coding of a first plurality of flip-flops, ~~whereby~~ each flip-
5 flop ~~has~~ having a data input to receive one of a first portion of bits
6 of said multiple bit test stimulus signal and a clock input to receive a
7 clocking signal to latch said first portion of the bits of the multiple bit
8 test stimulus signal;

9 a descriptive coding of a first plurality of multiplexor circuits, ~~whereby~~
10 each multiplexor circuit ~~has~~ having a first input to receive one of a
11 remaining portion of bits of said multiple bit test stimulus signal,
12 second input to receive an output of one of the first plurality of flip-
13 flops, and a select input to receive a loading signal to selectively
14 transfer the remaining bit of the multiple bit test stimulus signal and
15 the output of one of the first plurality of flip-flops to an output of said
16 multiplexor circuit;

17 a descriptive coding of a second plurality of flip-flops, ~~whereby~~ each
18 flip-flop of said plurality of flip-flops ~~has~~ having a data input
19 connected to an output of one of the first plurality of multiplexor
20 circuits, and a clock input connected to receive the clocking signal

21 to latch the output of one of the first plurality of multiplexor circuits
22 to the output of said flip-flop of said plurality of flip-flops; and
23 a descriptive coding of a second plurality of multiplexor circuits,
24 ~~whereby~~ each multiplexor circuit ~~has~~ having a first input connected
25 to a first flip-flop of the plurality of flip-flops, second input connected
26 to a second flip-flop of the second plurality of flip-flops, and a select
27 input connected to the clocking signal to alternately transfer the first
28 input to an output of said multiplexor circuits and the second input
29 to the output, as said clocking signal changes from a first level to a
30 second level and from the second level to the first level.

1 36. (Amended) The computer implemented hardware design system
2 ~~description coding~~ of claim 29 further comprising:
3 a descriptive coding of a test response comparison circuit connected to
4 said background and control decoder to receive an expected test
5 response signal providing a correct response expected from said
6 integrated circuits in response to said multiple bit test stimulus
7 signals, and connected to said integrated circuit to receive a test
8 response signal that is the response of the integrated circuit to said
9 multiple bit test stimulus signal.

1 37. (Amended) The computer implemented hardware design system
2 ~~description coding~~ of claim 36 wherein the descriptive coding of the test
3 response comparison circuit comprises:

4 a descriptive coding of a comparator circuit to receive the test
5 response signal and the expected test response signal, compare
6 said test response signal to said expected test response signal and
7 produce a test results signal indicating functioning of said
8 integrated circuits.

1 38. (Amended) The computer implemented hardware design system
2 ~~description coding~~ of claim 37 wherein said descriptive coding of
3 comparator circuit comprises:

4 descriptive coding of an exclusive OR and OR logic tree which
5 compares the ~~RAM data output from the serial-to-parallel converter~~
6 test response signal to an expected ~~data output pattern test~~
7 response signal from the background data.

1 39. (Amended) The computer implemented hardware design system
2 ~~description coding~~ of claim 37 wherein said descriptive coding of test
3 response comparison circuit further comprises:

4 a descriptive coding of an error-handling module to receive the test
5 response signal and the expected test response signal and creates

6 a diagnostic signal indicating a location of any fault determined to
7 exist within said integrated circuits.

1 40. (Amended) The computer implemented hardware design system
2 ~~description coding~~ of claim 39 wherein said descriptive coding of error
3 handling module comprises:

4 descriptive coding of a serial shift register composed of flip-flops, ~~which~~
5 that are presettable from the ~~serial to parallel data bus from the~~
6 RAM test response signal, and said serial shift register is being
7 loaded by the ~~PASS/FAIL~~ test result signal from the comparator,
8 and ~~whereby the~~ for transfer from a serial output from the shift
9 register ~~transfers the data for~~ diagnosis.

1 41. (Amended) The computer implemented hardware design system
2 ~~description coding~~ of claim 33 wherein said hardware description coding of
3 said test pattern generation and comparison apparatus requires the
4 number of bits of the multiple bit test stimulus signal and the adjusting in
5 time of the multiple bit test stimulus signal as parameters to automatically
6 create the physical description of said test pattern generation and
7 comparison apparatus during an automatic physical design of said
8 integrated circuit for placement on said semiconductor substrate.

1 42. (Amended) The computer implemented hardware design system
2 ~~description coding~~ of claim 29 wherein said functional integrated circuits

are selected from a group of functional integrated circuits consisting of logic circuits and memory array circuits.

43. (Amended) A data retention medium readable by a computer system containing a hardware description coding of a test pattern generation and comparison circuit, which, when executed, providing a description of a data retention medium to automatically creates a physical description of said data retention medium hardware description coding during an automatic physical design of said an integrated circuit for placement on said a semiconductor substrate, whereby said hardware description coding comprises comprising:

a descriptive coding of a background and command decoder connected to receive test background and command codes from said test controller, to translate said test background and command codes to multiple bit test stimulus signals that, when applied to said functional integrated circuits, create test response signals from said functional integrated circuits, ~~whereby said test stimulus signal has a plurality of bits; and~~

a descriptive coding of a plurality of latency buffers connected to said background and command decoder to receive said multiple bit test stimulus signals and to adjust in time the relationship of said

19 multiple bit test stimulus signals as required by said functional
20 integrated circuits.

1 44. (Amended) The data retention medium of claim 43 further comprising:

2 a descriptive coding of a plurality of parallel-to-serial converters
3 wherein each parallel-to-serial converter is connected to one of the
4 plurality of latency buffers, to convert said multiple bit test stimulus
5 to ~~[[a]]~~ serialized multiple bit test stimulus signals to be scanned to
6 a scan register of said functional integrated circuit.

1 45. (Amended) The data retention medium of claim 43 wherein said a
2 descriptive coding of background and command decoder comprises:

3 descriptive coding of a high level command bus decode logic ~~which~~
4 ~~decodes a high level command bus for activating RAM-control~~
5 ~~signals, and whereby the decode logic also controls the transfer of~~
6 ~~the background pattern for controlling transfer of a background~~
7 pattern of expected results to the error control module.

1 46. (Amended) The data retention medium of claim 43 wherein said a
2 descriptive coding of latency buffer comprises:

3 a descriptive coding of a plurality of serially connected flip-flop circuits,
4 ~~whereby~~ connected such that a first flip-flop circuit of said plurality
5 of serially connected flip-flop circuits has a data input connected to

6 said background and command decoder to receive one bit of said
7 multiple bit test stimulus signal and an output connected to a
8 subsequent flip-flop circuit of the serially connected flip-flop circuits,
9 ~~whereby~~ connected such that each subsequent flip-flop circuit of
10 the serially connected flip-flop circuits has an output connected to
11 the input of a following flip-flop circuit of said plurality of serially
12 connected flip-flop circuits, and ~~whereby~~ connected such that a last
13 flip-flop circuit has an input connected to an output of a previous
14 flip-flop circuit and an output containing a delayed bit of said
15 multiple bit test stimulus signal.

1 47. (Amended) The data retention medium of claim 46 ~~whereby~~ wherein the
2 adjusting in time of the multiple bit test stimulus signals is determined by a
3 number of flip-flop circuits in the plurality of serially connected flip-flop
4 circuits and the number of latency buffers of the plurality of latency buffers
5 is determined by a number of bits in the multiple bit test stimulus signals.

1 48. (Original) The data retention medium of claim 47 wherein the number of
2 flip-flop circuits is determined by the formula:

$$N = \frac{\lambda}{\phi}$$

where:

N is the number of said flip-flop circuits,

6 λ is the adjusting in time, and

7 ϕ is the period of the test access clocking

8 signal.

1 49. (Amended) The data retention medium of claim 44 wherein the parallel-to-
2 serial circuit comprises:

3 a descriptive coding of a first plurality of flip-flops, ~~whereby~~ each flip-
4 flop ~~has~~ having a data input to receive one of a first portion of bits
5 of said multiple bit test stimulus signal and a clock input to receive a
6 clocking signal to latch said first portion of the bits of the multiple bit
7 test stimulus signal;

8 a descriptive coding of a first plurality of multiplexor circuits, ~~whereby~~
9 each multiplexor circuit ~~has~~ having a first input to receive one of a
10 remaining portion of bits of said multiple bit test stimulus signal,
11 second input to receive an output of one of the first plurality of flip-
12 flops, and a select input to receive a loading signal to selectively
13 transfer the remaining bit of the multiple bit test stimulus signal and
14 the output of one of the first plurality of flip-flops to an output of said
15 multiplexor circuit;

16 a descriptive coding of a second plurality of flip-flops, ~~whereby~~ each
17 flip-flop of said plurality of flip-flops ~~has~~ having a data input

18 connected to an output of one of the first plurality of multiplexor
19 circuits, and a clock input connected to receive the clocking signal
20 to latch the output of one of the first plurality of multiplexor circuits
21 to the output of said flip-flop of said plurality of flip-flops; and
22 a descriptive coding of a second plurality of multiplexor circuits,
23 ~~whereby each multiplexor circuit has~~ having a first input connected
24 to a first flip-flop of the plurality of flip-flops, second input connected
25 to a second flip-flop of the second plurality of flip-flops, and a select
26 input connected to the clocking signal to alternately transfer the first
27 input to an output of said multiplexor circuits and the second input
28 to the output, as said clocking signal changes from a first level to a
29 second level and from the second level to the first level.

1 50. (Amended) The data retention medium of claim 43 further comprising:

2 a descriptive coding of a test response comparison circuit connected to
3 said background and control decoder to receive an expected test
4 response signal providing a correct response expected from said
5 integrated circuits in response to said multiple bit test stimulus
6 signals, and connected to said integrated circuit to receive a test
7 response signal that is the response of the integrated circuit to said
8 multiple bit test stimulus signal.

1 51. (Original) The data retention medium of claim 50 wherein the descriptive
2 coding of the test response comparison circuit comprises:

3 a descriptive coding of a comparator circuit to receive the test
4 response signal and the expected test response signal, compare
5 said test response signal to said expected test response signal and
6 produce a test results signal indicating functioning of said
7 integrated circuits.

1 52. (Amended) The data retention medium of claim 51 wherein said
2 descriptive coding of comparator circuit comprises:

3 descriptive coding of an exclusive OR and OR logic tree which
4 compares the ~~RAM data output from the serial to parallel converter~~
5 test response signal to an expected ~~data output pattern test~~
6 response signal from the background data.

1 53. (Amended) The data retention medium of claim 50 wherein said
2 descriptive coding of test response comparison circuit further comprises:

3 a descriptive coding of an error-handling module to receive the test
4 response signal and the expected test response signal and creates
5 a diagnostic signal indicating a location of any fault determined to
6 exist within said integrated circuits.

1 54. (Amended) The data retention medium of claim 53 wherein said
2 descriptive coding of error handling module comprises:
3 descriptive coding of a serial shift register composed of flip-flops, ~~which~~
4 ~~that~~ are presettable from the ~~serial to parallel data bus from the~~
5 ~~RAM test response signal, and said serial shift register is being~~
6 loaded by the ~~PASS/FAIL test result~~ signal from the comparator;
7 and ~~whereby the~~ for transfer from a serial output from of the serial
8 shift register ~~transfer the data for diagnosis.~~

1 55. (Amended) The data retention medium of claim 46 wherein said hardware
2 description coding of said test pattern generation and comparison
3 apparatus requires the number of bits of the multiple bit test stimulus
4 signal and the adjusting in time of the multiple bit test stimulus signal as
5 parameters to automatically create the physical description of said test
6 pattern generation and comparison apparatus during an automatic
7 physical design of said integrated circuit for placement on said
8 semiconductor substrate.

1 56. (Original) The data retention medium of claim 43 wherein said functional
2 integrated circuits are selected from a group of functional integrated
3 circuits consisting of logic circuits and memory array circuits.

1 57. (Amended) A method for generation of test patterns to be communicated
2 to integrated circuits and comparison of test response patterns

3 communicated from said integrated circuit to verify function of said
4 integrated circuits, comprising the steps of:

5 receiving a test pattern command indicating which tests ~~are to be~~
6 performed are communicated to said integrated circuit;

7 receiving a background pattern code indicating a pattern of multiple bit
8 test stimulus signals to be communicated to said integrated circuit;

9 decoding said test pattern command and said background pattern
10 code to create said multiple bit test stimulus signals;

11 adjusting a timing relation of said multiple bit test stimulus signals to
12 provide correct timing relationships for said multiple bit test stimulus
13 signals; and

14 communicating said multiple bit test stimulus signals to said integrated
15 circuit.

1 58. (Amended) The method of claim 57 further comprising the step of:

2 converting said multiple bit test stimulus signals to a serial test stimulus
3 signal;

1 59. (Amended) The method of claim 58 wherein communicating the serialized
2 multiple bit test stimulus signals comprises the step of:

3 scanning said serialized multiple bit test stimulus signals to a scan
4 register of said integrated circuit.

1 60. (Amended) The method of claim 58 wherein converting said multiple bit
2 test stimulus signals is accomplished in a parallel-to-parallelserial
3 converter comprising:

4 a first plurality of flip-flops, ~~whereby~~ each flip-flop ~~has~~ having a data
5 input to receive one of a first portion of bits of said multiple bit test
6 stimulus signal and a clock input to receive a clocking signal to
7 latch said first portion of the bits of the multiple bit test stimulus
8 signal;

9 a first plurality of multiplexor circuits, ~~whereby~~ each multiplexor circuit
10 ~~has~~ having a first input to receive one of a remaining portion of bits
11 of said multiple bit test stimulus signal, second input to receive an
12 output of one of the first plurality of flip-flops, and a select input to
13 receive a loading signal to selectively transfer the remaining bit of
14 the multiple bit test stimulus signal and the output of one of the first
15 plurality of flip-flops to an output of said multiplexor circuit;

16 a second plurality of flip-flops, ~~whereby~~ each flip-flop of said plurality of
17 flip-flops has a data input connected to an output of one of the first
18 plurality of multiplexor circuits, and a clock input connected to
19 receive the clocking signal to latch the output of one of the first

20 plurality of multiplexor circuits to the output of said flip-flop of said
21 plurality of flip-flops; and

22 a second plurality of multiplexor circuits, ~~whereby~~ each multiplexor
23 circuit ~~has~~ having a first input connected to a first flip-flop of the
24 plurality of flip-flops, second input connected to a second flip-flop of
25 the second plurality of flip-flops, and a select input connected to the
26 clocking signal to alternately transfer the first input to an output of
27 said multiplexor circuits and the second input to the output, as said
28 clocking signal changes from a first level to a second level and from
29 the second level to the first level.

1 61. (Amended) The method of claim 57 wherein adjusting the timing
2 relationship of said multiple bit test stimulus signals is accomplished in a
3 latency buffer comprising:

4 a plurality of serially connected flip-flop circuits, ~~whereby~~ connected
5 such that a first flip-flop circuit of said plurality of serially connected
6 flip-flop circuits has a data input connected to said background and
7 command decoder to receive one bit of said multiple bit test
8 stimulus signal and an output connected to a subsequent flip-flop
9 circuit of the serially connected flip-flop circuits, ~~whereby~~ connected
10 such that each subsequent flip-flop circuit of the serially connected
11 flip-flop circuits has an output connected to the input of a following

12 flip-flop circuit of said plurality of serially connected flip-flop circuits,
13 and ~~whereby~~ connected such that a last flip-flop circuit has an input
14 connected to an output of a previous flip-flop circuit and an output
15 containing a delayed bit of said multiple bit test stimulus signal.

1 62. (Amended) The method of claim 57 further comprising the steps of:

2 creating an expected test response signal from said test pattern
3 command and said background pattern code;

4 receiving the test response signals from the integrated circuit in
5 response to said multiple bit test stimulus signal;

6 comparing said test response signal to said expected test response
7 signal;

8 if said test response signal and expected test response signal indicate
9 said integrated circuit is functioning, communicating a favorable test
10 signal; and

11 if said test response signal and expected test response signal indicate
12 said integrated circuit is not functioning, communicating an
13 unfavorable test signal.

1 63. (Amended) The method of claim 61 wherein ~~said comparator~~ comparing
2 said test response signal is accomplished by a comparator comprising:

3 an exclusive OR and OR logic tree which compares the RAM
4 ~~data output from the serial to parallel converter~~ test response signal
5 to an expected ~~data output pattern~~ test response signal from the
6 background data.

1 64. (Amended) The method of claim 57 further comprising the step of:
2 converting said test response signal to a parallel test response signal
3 for comparison with the expected test response signal.

1 65. (Amended) The method of claim 64 wherein said converting is
2 accomplished by a serial-to-parallel conversion circuit comprising:
3 four flip-flops per serial input where connected such that the output of
4 the first flip-flop transfers to the second flip-flop and the third flip-
5 flop whose output is the second parallel bit and ~~whereby~~ the
6 second flip-flop transfers to the fourth flip-flop whose output is the
7 first parallel output bit.

1 66. (Original) The method of claim 64 further comprising the step of:
2 evaluating the comparison of the test response signal and the
3 expected test response signal to identify a fault location within said
4 integrated circuit if said test response signal and expected test
5 response signal indicate said integrated circuit is not functioning.

1 67. (Amended) The method of claim 66 where in said evaluating is
2 accomplished in an error handling module comprising:
3 a serial shift register composed of flip-flops, ~~which that~~ are presettable
4 from the ~~serial to parallel data bus from the RAM~~ test response
5 signal, and said serial shift register is loaded by the PASS/FAIL test
6 result signal from the comparator, ~~and whereby the~~ for transfer from
7 a serial output from of the serial shift register ~~transfer the data for~~
8 diagnosis.

1 68. (Original) The method of claim 57 wherein said functional integrated
2 circuits are selected from a group of integrated circuits consisting of logic
3 circuits and memory array circuits.